What is claimed is:

1. A method of adjusting a receiver clock duty cycle, comprising:

receiving a system clock signal;

detecting a duty cycle of a data signal;

comparing the detected duty cycle with a predetermined duty cycle in order to determine a first difference between the detected data signal duty cycle and the predetermined duty cycle;

generating a receiver clock from the system clock signal; and

adjusting a duty cycle of the receiver clock in accordance with the first difference between the detected data signal duty cycle and the predetermined duty cycle.

2. The method of claim 1, wherein

the step of detecting the duty cycle of a data signal comprises the detecting a first duty cycle of a first data signal from a first device, and detecting a second duty cycle of a second data signal from a second device;

the step of comparing the detected duty cycle with a predetermined duty cycle comprises comparing the first duty cycle with a first predetermined duty cycle in order to determine a first difference between the first duty cycle and the first predetermined duty cycle, and comparing the second duty cycle with a second predetermined duty cycle in order to determine a second difference between the second duty cycle and the second predetermined duty cycle; and

the step of adjusting a duty cycle of the receiver clock comprises adjusting a duty cycle of the receiver clock in accordance with the first difference when a receiver receives a data signal from the first device and adjusting the duty cycle of the receiver clock in accordance with the second difference when the receiver receives a data signal from the second device.

3. The method of claim 2, wherein the first and second data signals have signaling types which are different.

4. The method of claim 3, wherein the first and second predetermined duty cycles are different.

5. The method of claim 2, wherein the first and second devices are located on different integrated circuits.

6. The method of claim 1, including

detecting a duty cycle of the system clock signal;

comparing the duty cycle of the system clock signal with the predetermined duty cycle in order to determine a third difference between the detected system clock signal duty cycle and the predetermined duty cycle; and

adjusting the duty cycle of the receiver clock in accordance with the third difference.

7. The method of claim 6, wherein the third difference is less than about 10% of the predetermined duty cycle.

8. The method of claim 6, wherein the step of adjusting includes adjusting the duty cycle of the receiver clock such that a difference between the duty cycle of the receiver clock and the predetermined duty cycle is less than the third difference.

9. The method of claim 6, wherein the step of adjusting includes generating a duty cycle correction value based on the third difference and applying the duty cycle correction value to an amplifier circuit configured to alter the receiver clock signal duty cycle based on the duty cycle correction value.

10. The method of claim 9, wherein the duty cycle correction value determines which transistors are turned on in a binary-weighted set of transistors.

11. The method of claim 9, wherein the duty cycle correction value determines a voltage applied to a gate in a duty cycle correction circuit within the amplifier.

12. The method of claim 1, including processing the data signal using the duty cycle of the adjusted receiver clock.

13. The method of claim 1, wherein the predetermined duty cycle is 50%.

14. The method of claim 1, wherein the step of adjusting includes adjusting the duty cycle of the receiver clock such that a difference between the duty cycle of the receiver clock and the detected duty cycle of the data signal is less than the first difference.

15. The method of claim 1, wherein the step of adjusting includes generating a skew value based on the first difference and storing the skew value in a register.

16. The method of claim 15, further comprising applying the skew value to an amplifier circuit configured to alter the receiver clock signal duty cycle based on the skew value.

17. The method of claim 16, wherein the skew value determines which transistors are turned on in a binary-weighted set of transistors.

18. The method of claim 1, wherein the first difference is less than about 10% of the predetermined duty cycle.

19. The method of claim 1, wherein the method is performed by an integrated circuit and the data signal is received from a module with the integrated circuit.

20. The method of claim 1, wherein the method is performed by a first integrated circuit and the data signal is received from another integrated circuit.

21. An integrated circuit, comprising:

a clock receiver configured to receive a system clock signal having a duty cycle;

a data signal duty cycle detector configured to detect a first duty cycle of a first data signal and to generate a first difference signal representing a difference between the first duty cycle and a first predetermined duty cycle; and

a receiver clock generator configured to output a receiver clock signal based on the system clock signal and the first difference signal, the receiver clock generator including a first correction circuit configured to adjust a duty cycle of the receiver clock signal in accordance with the first difference signal.

22. The integrated circuit of claim 21, wherein the data signal duty cycle detector is further configured to detect a second duty cycle of a second data signal and to generate a second difference signal representing a difference between the second data signal duty cycle and a second predetermined duty cycle; the first data signal has a first data signal type, the second data signal has a second data signal type, and the receiver clock generator is further configured to output a first receiver clock signal based on the system clock signal and the first difference signal when a receiver receives a data signal of the first data signal type and to

output a second receiver clock signal based on the system clock signal and the second difference signal when the receiver receivers a data signal of the second data signal type.

23. The integrated circuit of claim 22, wherein the first and second data signaling types are different.

24. The integrated circuit of claim 23, wherein the first and second predetermined duty cycles are different.

25. The integrated circuit of claim 22, wherein data signals of the first data signaling type are from a first device and data signals of the second signal type are from a second device.

26. The integrated circuit of claim 25, wherein the first and second devices are located on different integrated circuits.

27. The integrated circuit of claim 21, including

a clock cycle detector configured to detect a duty cycle of the system clock signal and to generate a third difference signal representing a difference between the detected system clock signal duty cycle and the first predetermined duty cycle; and

a second correction circuit configured to adjust the duty cycle of the receiver clock signal in accordance with the third difference signal.

28. The integrated circuit of claim 27, wherein the third difference is less than about 10% of the predetermined duty cycle.

29. The integrated circuit of claim 27, wherein the second correction circuit adjusts the duty cycle of the receiver clock such that a difference between the duty cycle of the receiver clock and the predetermined duty cycle is less than the third difference.

30. The integrated circuit of claim 27, wherein the duty cycle correction value is applied to an amplifier circuit configured to alter the receiver clock signal duty cycle based on the duty cycle correction value.

31. The integrated circuit of claim 30, wherein the duty cycle correction value determines which transistors are turned on in a binary-weighted set of transistors.

32. The integrated circuit of claim 30, wherein the duty cycle correction value determines a voltage applied to a gate in a duty cycle correction circuit within the amplifier.

33. The integrated circuit of claim 21, including a detector configured to process the data signal using the duty cycle of the adjusted receiver clock signal.

34. The integrated circuit of claim 21, wherein the predetermined duty cycle is 50%.

35. The integrated circuit of claim 21, wherein the first correction circuit adjusts the duty cycle of the receiver clock such that a difference between the duty cycle of the receiver clock and the first duty cycle is less than the first difference.

36. The integrated circuit of claim 21, wherein the data signal duty cycle detector generates a duty cycle correction value based on the first difference and stores the duty cycle correction value in a register.

37. The integrated circuit of claim 36, wherein the duty cycle correction value is applied to an amplifier circuit configured to alter the receiver clock signal duty cycle based on the duty cycle correction value.

38. The integrated circuit of claim 37, wherein the duty cycle correction value determines which transistors are turned on in a binary-weighted set of transistors within the amplifier circuit.

39. The integrated circuit of claim 21, wherein the first difference is less than about 10% of the predetermined duty cycle.

40. The integrated circuit of claim 21, wherein the first data signal is received from a module within the integrated circuit.

41. The integrated circuit of claim 21, wherein the first data signal is received from another integrated circuit.

42. An integrated circuit, comprising:

means for receiving a system clock signal having a duty cycle;

means for detecting a duty cycle of a data signal and for generating a first difference signal representing a difference between the detected data signal duty cycle and a predetermined duty cycle; and

means for generating a receiver clock signal based on the system clock signal and the first difference signal, including means for adjusting a duty cycle of the receiver clock signal in accordance with the first difference signal.